CLAIMS

What is claimed is:

1. A method for manufacturing a flash memory device, said method comprising:

providing a semiconductor substrate;

forming a gate oxide layer on said semiconductor substrate;

forming a first semiconductor layer on said gate oxide layer;

forming an insulating layer on said first semiconductor layer;

removing partial said insulating layer until said partial first semiconductor layer is exposed;

forming a semiconductor spacer on both said insulating layer and said first semiconductor layer;

removing partial said semiconductor spacer until said insulating layer is exposed;

removing said insulating layer until said first semiconductor layer is exposed, wherein said semiconductor spacer protrudes through the top surface of said first semiconductor layer;

forming an insulating stacked structure on said first semiconductor layer and said semiconductor spacer; and

forming a second semiconductor layer on said insulating stacked structure.

2. The method for manufacturing a flash memory device according to claim 1, further comprising removing partial said first semiconductor layer, wherein said insulating layer is used as an etching mask.

3. The method for manufacturing a flash memory device according to claim 2,

further comprising forming said semiconductor spacer on the side wall of said first semiconductor layer.

4. The method for manufacturing a flash memory device according to claim 2, wherein removing partial said first semiconductor layer is conducted by an etching process.

5. The method for manufacturing a flash memory device according to claim 1, further comprising removing said first semiconductor layer to expose said gate oxide layer, wherein said insulating layer is used as an etching mask.

6. The method for manufacturing a flash memory device according to claim 5, further comprising forming said semiconductor spacer on said gate oxide layer.

7. The method for manufacturing a flash memory device according to claim 1, wherein said semiconductor substrate is of silicon material.

8. The method for manufacturing a flash memory device according to claim 1, wherein said semiconductor spacer is of polysilicon material.

9. The method for manufacturing a flash memory device according to claim 1, wherein said first semiconductor layer is of polysilicon material.

10. The method for manufacturing a flash memory device according to claim 1, wherein said second semiconductor layer is of polysilicon material.

11. The method for manufacturing a flash memory device according to claim 1, wherein said insulating layer is of silicon nitride material.

12. The method for manufacturing a flash memory device according to claim 1, wherein said first semiconductor layer and said semiconductor spacer together form a floating gate.

13. The method for manufacturing a flash memory device according to claim 1, wherein said second semiconductor layer forms a control gate.

14. The method for manufacturing a flash memory device according to claim 1, wherein said gate oxide layer is of silicon dioxide (SiO_2) material.

15. The method for manufacturing a flash memory device according to claim 1, wherein said insulating stacked structure is of oxide-nitride-oxide stacked structure.

16. The method for manufacturing a flash memory device according to claim 1, wherein said semiconductor spacer can be used as an etching mask in a self-aligned etching process.

17. The method for manufacturing a flash memory device according to claim 1, wherein said steps of removing partial said insulating layer comprises:

forming a photo resist layer on said insulating layer;

patterning said photo resist layer; and

using said patterned photo resist layer to etch away partial said insulating

layer.

18. A flash memory device structure to enhance the gate coupling ratio, said structure comprising:

a semiconductor substrate;

a gate oxide layer on said semiconductor substrate;

a first semiconductor layer on said gate oxide layer;

a semiconductor spacer protruding through the top surface of said first semiconductor layer;

an insulating stacked structure over both the surface of said first semiconductor layer and said semiconductor spacer; and

a second semiconductor layer on said insulating stacked structure.

19. A flash memory device structure to enhance the gate coupling ratio according to claim 18, wherein said semiconductor substrate is of silicon material.

20. A flash memory device structure to enhance the gate coupling ratio according to claim 18, wherein said semiconductor spacer and said first semiconductor layer are configured for constituting a floating gate.

21. A flash memory device structure to enhance the gate coupling ratio according to claim 18, wherein said second semiconductor layer is used as a control gate.

22. A flash memory device structure to enhance the gate coupling ratio

according to claim 18, wherein said insulating stacked structure is an oxide-nitride-oxide stacked structure.

5